UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/524,571	02/15/2005	Igor Ivanovich Blednov	NL 020752	8310

24737 7590 08/03/2005

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
LEE, JOHN D	

ART UNIT	PAPER NUMBER
2874	

DATE MAILED: 08/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/524,571	BLEDNOV, IGOR IVANOVICH	
	Examiner	Art Unit	
	John D. Lee	2874	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-10 and 12-18 is/are rejected.

7)☒ Claim(s) 11 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 15 February 2005 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 0205.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

A certified copy of the European priority document relied upon in this National Stage application has been received from the International Bureau (PCT Rule 17.2(a)).

The thirteen (13) sheets of drawings filed in this application are acceptable.

The disclosure has not been studied to the extent necessary to discover all possible minor errors therein. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claims 14, 15, and 18 are objected to because of the following minor informalities. Appropriate correction is required. In claim 14, it is unclear which transistor is being referenced. Is it *both* transistors? In claim 15, there is no antecedent support for "the compensation circuit"; it is thus believed that claim 15 should depend from claim 14 rather than from claim 12. Claim 18 appears to set forth a general description of capacitance and does not clearly describe how this relates to (or further limits) the package of claim 12.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10, 12-15, and 18 are rejected under 35 U.S.C. § 102(b) as being clearly anticipated by U.S. Patent 6,320,462 to Alley. Alley discloses a high power Doherty amplifier circuit having an input terminal **10a** and an output terminal **10b** comprising: a carrier transistor amplifying stage **20**; a peak transistor amplifying stage **24**; a first input line **12a, 14a** connecting the input terminal to an input of the carrier amplifier; a second input line **12b, 16a** connecting the input terminal to an input of the peak amplifier; a first output line **20b, 21a, 21c** connecting the

output terminal to an output of the carrier amplifier; and a second output line **24b, 34a, 34b, 16b, 21b, 21c** connecting the output terminal to an output of the peak amplifier. As seen in Figure 5, Alley also discloses such a high power Doherty amplifier circuit in a package with support structure supporting each of the circuit elements. In the description of Figure 5, Alley explains that the first and second input lines, as well as the first and second output lines, include serial and/or parallel circuits of capacitance and inductance. These output connections are "compensation" circuits. Regarding claim 8, it is noted that the Alley carrier transistor and peak transistor have individual transconductance parameters and threshold voltage values (regardless of what numerical value (even zero) that the parameters and values may assume).

Claims 1 and 5-8 are further rejected under 35 U.S.C. § 102(b) as being clearly anticipated by U.S. Patent 6,469,581 to Kobayashi. Kobayashi discloses a high power Doherty amplifier circuit having an input terminal **34** and an output terminal (unnumbered) comprising: a carrier transistor amplifying stage **22**; a peak transistor amplifying stage **24**; a first input line connecting the input terminal to an input of the carrier amplifier; a second input line connecting the input terminal to an input of the peak amplifier; a first output line connecting the output terminal to an output of the carrier amplifier; and a second output line connecting the output terminal to an output of the peak amplifier. As explained in column 4, lines 42-56, the first and second output lines of Kobayashi can comprise elements of inductance and/or capacitance. Regarding claim 8, it is noted that the Kobayashi carrier transistor and peak transistor have individual transconductance parameters and threshold voltage values (regardless of what numerical value (even zero) that the parameters and values may assume).

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16 and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,320,462 to Alley. As explained above, Alley discloses the basic claimed high power Doherty amplifier circuit. In discussing the various lines and inductances, however, Alley does not use the word "wires". Since this is the most common implementation known in the art, it would have been obvious to the person of ordinary skill to have used "bond wires" of appropriate length for the inductances and input lines of the Alley amplifier circuit.

Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Alley and Kobayashi, the closest prior art documents of record, do not disclose or suggest a control circuit connected to the carrier transistor amplifying stage and the peak transistor amplifying stage for providing desired dynamic control of amplification class parameters of the transistors.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent 6,853,245 to Kim et al describes another Doherty amplifier known in the art.

All of the prior art documents cited by applicant in the Information Disclosure Statement filed on February 15, 2005, have been considered and made of record. Note the attached initialed copy of form PTO-1449.

Any inquiry concerning the merits of this communication should be directed to Examiner John D. Lee at telephone number (571) 272-2351. The Examiner's normal work schedule is Tuesday through Friday, 6:30 AM to 5:00 PM. Any inquiry of a general or clerical nature (i.e. a request for a missing form or paper, etc.) should be directed to the Technology Center 2800 receptionist at telephone number (571) 272-1562, to the technical support staff supervisor (Team 8) at telephone number (571) 272-1564, or to the Technology Center 2800 Customer Service Office at telephone number (571) 272-1626.

John D. Lee

John D. Lee
Primary Patent Examiner
Group Art Unit 2874